HEWLETT-PACKARD COMPANY
Intellectual Property Administration
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PATENT APPLICATION

ATTORNEY DOCKET NO. 200308581-1

IN THE
UNITED STATES PATENT AND TRADEMARK OFFICE

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|---|---|---|---|
| Inventor(s): | Andrew H. Barr et al. | Confirmation No.: | 3950 |
| Application No.: | 10/714,386 | Examiner: | Aditya S. Bhat |
| Filing Date: | Nov. 14, 2003 | Group Art Unit: | 2863 |

Title: SYSTEM AND METHOD FOR TESTING A MEMORY WITH AN EXPANSION CARD USING DMA

Mail Stop Appeal Brief-Patents
Commissioner For Patents
PO Box 1450
Alexandria, VA 22313-1450

## TRANSMITTAL OF APPEAL BRIEF

Transmitted herewith is the Appeal Brief in this application with respect to the Notice of Appeal filed on Feb. 21, 2008.

☒ The fee for filing this Appeal Brief is $ 10.00 (37 CFR 41.20).

☐ No Additional Fee Required.

NOTE: A fee of $500 was charged for the Appeal Brief filed November 13, 2006. Please charge the different of $10.00 between the current fee of $510 and the previously paid fee of $500.

**(complete (a) or (b) as applicable)**

The proceedings herein are for a patent application and the provisions of 37 CFR 1.136(a) apply.

☐ (a) Applicant petitions for an extension of time under 37 CFR 1.136 (fees: 37 CFR 1.17(a)-(d)) for the total number of months checked below:

| | | | |
|---|---|---|---|
| ☐ 1st Month $120 | ☐ 2nd Month $460 | ☐ 3rd Month $1050 | ☐ 4th Month $1640 |

☒ The extension fee has already been filed in this application.

☐ (b) Applicant believes that no extension of time is required. However, this conditional petition is being made to provide for the possibility that applicant has inadvertently overlooked the need for a petition and fee for extension of time.

Please charge to Deposit Account 08-2025 the sum of $ 10. At any time during the pendency of this application, please charge any fees required or credit any over payment to Deposit Account 08-2025 pursuant to 37 CFR 1.25. Additionally please charge any fees to Deposit Account 08-2025 under 37 CFR 1.16 through 1.21 inclusive, and any other sections in Title 37 of the Code of Federal Regulations that may regulate fees.

Respectfully submitted,

Andrew H. Barr et al.

By /Christopher P. Kosh/

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Date : May 20, 2008

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**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

**BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES**

| | | |
|---|---|---|
| Applicant: | Andrew H. Barr et al. | Examiner: Aditya S. Bhat |
| Serial No.: | 10/714,386 | Group Art Unit: 2863 |
| Filed: | Nov. 14, 2003 | Docket No.: 200308581-1 |
| Title: | SYSTEM AND METHOD FOR TESTING A MEMORY WITH AN EXPANSION CARD USING DMA | |

## APPEAL BRIEF UNDER 37 C.F.R. §41.37

**Mail Stop Appeal Brief – Patents**
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir/Madam:

This Appeal Brief is submitted in support of the Notice of Appeal filed on February 21, 2008, appealing the final rejection of claims 1-20 of the above-identified application as set forth in the Final Office Action mailed January 11, 2008.

The U.S. Patent and Trademark Office is hereby authorized to charge Deposit Account No. 08-2025 in the amount of $10.00[1] for filing a Brief in Support of an Appeal as set forth under 37 C.F.R. §41.20(b)(2). At any time during the pendency of this application, please charge any required fees or credit any overpayment to Deposit Account No. 08-2025.

Appellant respectfully requests consideration and reversal of the Examiner's rejection of pending claims 1-20.

[1] A fee of $500 was charged for the Appeal Brief filed November 13, 2006. Accordingly, please charge the difference of $10.00 between the current fee for filing an Appeal Brief ($510.00) and the amount previously paid ($500.00).

## TABLE OF CONTENTS

## REAL PARTY IN INTEREST

The real party in interest is Hewlett-Packard Development Company, LP having a principal place of business at 20555 S.H. 249 Houston, TX 77070, U.S.A. (hereinafter "HPDC"). HPDC is a Texas limited partnership and is a wholly-owned affiliate of Hewlett-Packard Company, a Delaware corporation, headquartered in Palo Alto, CA. The general or managing partner of HPDC is HPQ Holdings, LLC.

## RELATED APPEALS AND INTERFERENCES

There are no other appeals or interferences known to Appellant that will have a bearing on the Board's decision in the present Appeal.

## STATUS OF CLAIMS

In a Final Office Action mailed January 11, 2008, claims 1-20 were finally rejected. Claims 1-20 are pending in the application, and are the subject of the present Appeal.

## STATUS OF AMENDMENTS

No amendments have been entered subsequent to the Final Office Action mailed January 11, 2008.

## SUMMARY OF THE CLAIMED SUBJECT MATTER

The Summary is set forth as an exemplary embodiment as the language corresponding to independent claims 1-20. Discussions about elements of claims 1-20 can be found at least at the cited locations in the specification and drawings.

Independent claim 1 claims a computer system (p. 3, lines 3-26; Fig. 1, reference number 100; Fig. 4, reference number 100). The computer system comprises a processor configured to execute an operating system (p. 3, line 27 to p. 4, line 3; Fig. 1, reference number 110; Fig. 4, reference number 110), a memory controller coupled to the processor (p. 4, lines 4-10; Fig. 1, reference number 122; Fig. 2, reference number 122; Fig. 4, reference number 428), a memory coupled to the memory controller (p. 4, lines 20-24; Fig. 1, reference number 130; Fig. 2, reference number 130; Fig. 4, reference number 130), a first input/output (I/O) controller coupled to the memory controller (p. 4, lines 25-31; Fig. 1, reference number 130; Fig. 2, reference number 130; Fig. 4, reference number 130), a first expansion slot coupled to the first I/O controller (p. 4, lines 25-31; Fig. 1, reference number 130; Fig. 2, reference number 130; Fig. 4, reference number 130), and a test module card directly coupled to the first expansion slot (p. 5, lines 1-15; Fig. 1, reference number 150; Fig. 2, reference number 150; Fig. 4, reference number 150). The test module card is configured to obtain access to a portion of the memory from the operating system (p. 6, lines 9-17; Fig. 3, reference number 302), and the test module card is configured to cause tests to be performed on the portion of the memory using direct memory access (DMA) subsequent to obtaining access to the portion of the memory (p. 5, line 1 to p. 6, line 31; Fig. 3, reference number 304).

Independent claim 9 claims a method. The method comprises obtaining access to a portion of a memory of a computer system from an operating system during operation of a computer system (p. 6, lines 9-17; Fig. 3, reference number 302), generating a test transaction in a test module card directly coupled to an expansion slot of the computer system, and providing the test transaction to the portion using direct memory access (DMA) to cause information to be read from or stored into the portion subsequent to obtaining access to the portion of the memory (p. 5, line 1 to p. 6, line 31; Fig. 3, reference number 304).

Independent claim 15 claims a computer system (p. 3, lines 3-26; Fig. 1, reference number 100; Fig. 4, reference number 100). The computer system comprises a processor (p. p. 4, lines 4-10; Fig. 1, reference number 122; Fig. 2, reference number 122; Fig. 4, reference number 428), a memory controller coupled to the processor and configured to perform error correction (p. 4, lines 4-10; Fig. 1, reference number 122; Fig. 2, reference number 122; Fig. 4, reference number 428), a memory coupled to the memory controller (p. 4, lines 20-24; Fig. 1, reference number 130; Fig. 2, reference number 130; Fig. 4, reference number 130), an input/output (I/O) controller coupled to the memory controller (p. 4, lines 25-31; Fig. 1, reference number 130; Fig. 2, reference number 130; Fig. 4, reference number 130), an expansion slot coupled to the I/O controller (p. 4, lines 25-31; Fig. 1, reference number 130; Fig. 2, reference number 130; Fig. 4, reference number 130), and a test module card directly coupled to the expansion slot (p. 5, lines 1-15; Fig. 1, reference number 150; Fig. 2, reference number 150; Fig. 4, reference number 150). The test module card is configured to obtain access to a portion of the memory from an operating system (p. 6, lines 9-17; Fig. 3, reference number 302), and the test module card is configured to cause tests to be performed on the portion of the memory by providing read transactions associated with the memory to the I/O controller subsequent to obtaining access to the portion of the memory (p. 5, line 1 to p. 6, line 31; Fig. 3, reference number 304).

## GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Claims 1-20 stand rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent Publication No. 2003/0115385 (Adamane).[2]

[2] Applicants respectfully note that Adamane was cited by Applicants in an Information Disclosure Statement filed concurrently with the filing of the present application. Adamane was fully considered by the Examiner as evidenced by the Examiner's initials and signature on Form PTO-1449 dated February 25, 2005.

A rejection based on Adamane was not included in Office Actions mailed March 4, 2005, August 15, 2005, December 16, 2005, May 18, 2006, and March 5, 2007.

Applicants filed an Appeal Brief appealing the rejections presented in the Office Action mailed May 18, 2006.

Claims 1-8 and 15-20 were allowed in the Office Action mailed March 5, 2007 (i.e., the first Office Action subsequent to the Appeal Brief).

Subsequent to the indication of that claims 1-8 and 15-20 were allowed, an Office Action mailed August 6, 2007 included the rejection based on Adamane. The Final Office Action mailed January 11, 2008 repeated the rejection based on Adamane.

## ARGUMENT

### I. The Applicable Law

The Examiner has the burden under 35 U.S.C. §103 to establish a *prima facie* case of obviousness. *In re Fine,* 837 F.2d 1071, 1074, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988). Three criteria must be satisfied to establish a *prima facie* case of obviousness. First, the Examiner must show that some objective teaching in the prior art or some knowledge generally available to one of ordinary skill in the art would teach, suggest, or motivate one to modify a reference or to combine the teachings of multiple references. *Id.* Second, the prior art can be modified or combined only so long as there is a reasonable expectation of success. *In re Merck & Co., Inc.,* 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). Third, the prior art reference or combined prior art references must teach or suggest all of the claim limitations. *In re Royka,* 490 F.2d 981, 180 USPQ 580 (CCPA 1974). These three criteria are also set forth in §706.02(j) of the M.P.E.P.

### II. Rejection of Claims 1-20 under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent Publication No. 2003/0115385 (Adamane)

Adamane does not teach or suggest all of the limitations of claims 1-20.

#### A. Rejection of Claims 1-8 under 35 U.S.C. §103(a) as being unpatentable over Adamane

Claim 1 recites, *inter alia*:

> a processor configured to execute an operating system;
> a memory controller coupled to the processor;
> a memory coupled to the memory controller;
> a first input/output (I/O) controller coupled to the memory controller;
> a first expansion slot coupled to the first I/O controller; and
> a test module card directly coupled to the first expansion slot;
> wherein the test module card is configured to obtain access to a portion of the memory from the operating system, and wherein the test module card is configured to cause tests to be performed on the portion of the memory using direct memory access (DMA) subsequent to obtaining access to the portion of the memory.

Adamane does not teach or suggest "a test module card directly coupled to the first expansion slot", "wherein the test module card is configured to obtain access to a portion of the memory from the operating system" or "wherein the test module card is configured to cause tests to be performed on the portion of the memory using direct memory access (DMA) subsequent to obtaining access to the portion of the memory" as recited in claim 1.

The Examiner plainly concedes that "Adamane et al (sic) does not appear to explicitly teach a test module card." Final Office Action mailed January 11, 2008, p. 7 (hereafter Final Office Action).

The Examiner, however, attempts to overcome this deficiency by citing "I/O cards" in the BACKGROUND OF THE INVENTION section of Adamane (paragraph [0004]) and "testing a (sic) I/O device" in paragraph [0015] of Adamane. Final Office Action, pp. 7-8.

In paragraph [0015], Adamane teaches that:

> I/O devices 118 are testing devices that stress test computer system 100 by performing a series of direct memory access (DMA) transfers of blocks of memory to and from cache memory 104 (and by implication main memory 106). I/O devices 118 perform repeated DMA transfers while varying transfer parameters pseudo-randomly so as to simulate the behavior of many different types of I/O devices. Also, processors 101 may also access cache memory 104 concurrently, so as to place further stress on computer system 100. The resulting contents of cache memory 104 and/or main memory 106 can then be examined to observe the effects of varying DMA parameters and concurrent memory access between I/O devices 118 and processors 101.

These teachings of Adamane, even when combined with the teachings in the BACKGROUND OF THE INVENTION section of Adamane, do not teach or suggest "a test module card directly coupled to the first expansion slot" as recited in claim 1.

In addition, Adamane does not teach or suggest "wherein the test module card is configured to obtain access to a portion of the memory from the operating system" as recited in claim 1. The Examiner also cites paragraph [0015] of Adamane as a teaching of this feature of claim 1. Final Office Action, p. 2. Paragraph [0015] of Adamane, however, does not describe any interaction between a test module card and an operating system.

The Examiner attempts to overcome this further deficiency by referencing, without citation or listing in the Notice of References Cited (PTO-892), "Merriam Websters's online dictionary" and alleging "it would be obvious for the I/O card and the operating system to interact." Final Office Action, p. 8. This reference and allegation does not amount to a teaching or suggestion by Adamane of "wherein the test module card is configured to obtain access to a portion of the memory from the operating system" as recited in claim 1.

Further, Adamane further does not teach or suggest "wherein the test module card is configured *to cause tests to be performed on the portion of the memory* using direct memory access (DMA) subsequent to obtaining access to the portion of the memory" as recited in claim 1 (emphasis added). The Examiner cites paragraph [0015] of Adamane as a teaching of this feature of claim 1. Final Office Action, p. 2. Paragraph [0015] of Adamane, however, does not support that notion that tests are "performed on the portion of the memory" as recited in claim 1. Instead, Adamane teaches away from this feature of claim 1 by teaching that "[t]he present invention provides a method, computer program product, input/output device, and computer system for stress testing the I/O subsystem of a computer system." Adamane, paragraph [0005], lines 1-3.

Adamane does not teach or suggest the above features of claim 1. Accordingly, Applicants respectfully request the reversal of the rejection of claim 1 and claims 2-8 which depend from claim 1 under 35 U.S.C. §103(a) for at least this reason.

### B. Rejection of Claims 9-14 under 35 U.S.C. §103(a) as being unpatentable over Adamane

Claim 9 recites, *inter alia*:

> obtaining access to a portion of a memory of a computer system from an operating system during operation of a computer system;
>
> generating a test transaction in a test module card directly coupled to an expansion slot of the computer system; and
>
> providing the test transaction to the portion using direct memory access (DMA) to cause information to be read from or stored into the portion subsequent to obtaining access to the portion of the memory.

Adamane does not teach or suggest "obtaining access to a portion of a memory of a computer system from an operating system during operation of a computer system" as recited in claim 9. The Examiner cites paragraph [0015] of Adamane as a teaching of this feature of claim 9. Final Office Action, p. 4. Paragraph [0015] of Adamane, however, does not describe any interaction between a test module card and an operating system.

The Examiner attempts to overcome this further deficiency by referencing, without citation or listing in the Notice of References Cited (PTO-892), "Merriam Websters's online dictionary" and alleging "it would be obvious for the I/O card and the operating system to interact." Final Office Action, p. 8. This reference and allegation does not amount to a teaching or suggestion by Adamane of "obtaining access to a portion of a memory of a computer system from an operating system during operation of a computer system" as recited in claim 9.

The Examiner plainly concedes that "Adamane et al (sic) does not appear to explicitly teach a test module card." Final Office Action mailed January 11, 2008, p. 7 (hereafter Final Office Action).

The Examiner, however, attempts to overcome this deficiency by citing "I/O cards" in the BACKGROUND OF THE INVENTION section of Adamane (paragraph [0004]) and "testing a (sic) I/O device" in paragraph [0015] of Adamane. Final Office Action, pp. 7-8.

In paragraph [0015], Adamane teaches that:

> I/O devices 118 are testing devices that stress test computer system 100 by performing a series of direct memory access (DMA) transfers of blocks of memory to and from cache memory 104 (and by implication main memory 106). I/O devices 118 perform repeated DMA transfers while varying transfer parameters pseudo-randomly so as to simulate the behavior of many different types of I/O devices. Also, processors 101 may also access cache memory 104 concurrently, so as to place further stress on computer system 100. The resulting contents of cache memory 104 and/or main memory 106 can then be examined to observe the effects of varying DMA parameters and concurrent memory access between I/O devices 118 and processors 101.

These teachings of Adamane, even when combined with the teachings in the BACKGROUND OF THE INVENTION section of Adamane, do not teach or suggest "generating a test transaction in a test module card directly coupled to an expansion slot of the computer system" as recited in claim 9.

Adamane does not teach or suggest the above features of claim 9. Accordingly, Applicants respectfully request the reversal of the rejection of claim 9 and claims 10-14 which depend from claim 9 under 35 U.S.C. §103(a) for at least this reason.

### C. Rejection of Claims 15-20 under 35 U.S.C. §103(a) as being unpatentable over Adamane

Claim 15 recites, *inter alia*:

> a processor;
> a memory controller coupled to the processor and configured to perform error correction;
> a memory coupled to the memory controller;
> an input/output (I/O) controller coupled to the memory controller;
> an expansion slot coupled to the I/O controller; and
> a test module card directly coupled to the expansion slot;
> wherein the test module card is configured to obtain access to a portion of the memory from an operating system, and wherein the test module card is configured to cause tests to be performed on the portion of the memory by providing read transactions associated with the memory to the I/O controller subsequent to obtaining access to the portion of the memory.

Adamane does not teach or suggest "a test module card directly coupled to the expansion slot", "wherein the test module card is configured to obtain access to a portion of the memory from an operating system", or "wherein the test module card is configured to cause tests to be performed on the portion of the memory by providing read transactions associated with the memory to the I/O controller subsequent to obtaining access to the portion of the memory" as recited in claim 15.

The Examiner plainly concedes that "Adamane et al (sic) does not appear to explicitly teach a test module card." Final Office Action mailed January 11, 2008, p. 7 (hereafter Final Office Action).

The Examiner, however, attempts to overcome this deficiency by citing "I/O cards" in the BACKGROUND OF THE INVENTION section of Adamane (paragraph [0004]) and "testing a (sic) I/O device" in paragraph [0015] of Adamane. Final Office Action, pp. 7-8.

In paragraph [0015], Adamane teaches that:

> I/O devices 118 are testing devices that stress test computer system 100 by performing a series of direct memory access (DMA) transfers of blocks of memory to and from cache memory 104 (and by implication main memory 106). I/O devices 118 perform repeated DMA transfers while varying transfer parameters pseudo-randomly so as to simulate the behavior of many different types of I/O devices. Also, processors 101 may also access cache memory 104 concurrently, so as to place further stress on computer system 100. The resulting contents of cache memory 104 and/or main memory 106 can then be examined to observe the effects of varying DMA parameters and concurrent memory access between I/O devices 118 and processors 101.

These teachings of Adamane, even when combined with the teachings in the BACKGROUND OF THE INVENTION section of Adamane, do not teach or suggest "a test module card directly coupled to the first expansion slot" as recited in claim 15.

In addition, Adamane does not teach or suggest "wherein the test module card is configured to obtain access to a portion of the memory from an operating system" as recited in claim 15. The Examiner cites paragraph [0015] of Adamane as a teaching of this feature

of claim 15. Final Office Action, p. 6. Paragraph [0015] of Adamane, however, does not describe any interaction between a test module card and an operating system.

The Examiner attempts to overcome this further deficiency by referencing, without citation or listing in the Notice of References Cited (PTO-892), "Merriam Websters's online dictionary" and alleging "it would be obvious for the I/O card and the operating system to interact." Final Office Action, p. 8. This reference and allegation does not amount to a teaching or suggestion by Adamane of "wherein the test module card is configured to obtain access to a portion of the memory from the operating system" as recited in claim 15.

Further, Adamane further does not teach or suggest "wherein the test module card is configured *to cause tests to be performed on the portion of the memory* by providing read transactions associated with the memory to the I/O controller subsequent to obtaining access to the portion of the memory" as recited in claim 15 (emphasis added). The Examiner again cites paragraph [0015] of Adamane as a teaching of this feature of claim 15. Final Office Action, p. 6. Paragraph [0015] of Adamane, however, does not support that notion that tests are "performed on the portion of the memory" as recited in claim 15. Instead, Adamane teaches away from this feature of claim 15 by teaching that "[t]he present invention provides a method, computer program product, input/output device, and computer system for stress testing the I/O subsystem of a computer system." Adamane, paragraph [0005], lines 1-3.

Adamane does not teach or suggest the above features of claim 15. Accordingly, Applicants respectfully request the reversal of the rejection of claim 15 and claims 16-20 which depend from claim 15 under 35 U.S.C. §103(a) for at least this reason.

## CONCLUSION

For the above reasons, Appellants respectfully submit that claims 1-20 of the pending Application have not been established to be obvious in view of the cited reference. Accordingly, Appellants respectfully request that the Examiner be reversed.

Any inquiry regarding this Amendment and Response should be directed to either Christopher P. Kosh at Telephone No. (512) 241-2403, Facsimile No. (512) 241-2409 or David A. Plettner at Telephone No. (408) 447-3013, Facsimile No. (408) 447-0854. In addition, all correspondence should continue to be directed to the following address:

**Hewlett-Packard Company**
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Respectfully submitted,

Andrew W. Barr et al.,

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Date: May 20, 2008

CPK:dmd

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## CLAIMS APPENDIX

1. (Previously Presented) A computer system comprising:

a processor configured to execute an operating system;

a memory controller coupled to the processor;

a memory coupled to the memory controller;

a first input/output (I/O) controller coupled to the memory controller;

a first expansion slot coupled to the first I/O controller; and

a test module card directly coupled to the first expansion slot;

wherein the test module card is configured to obtain access to a portion of the memory from the operating system, and wherein the test module card is configured to cause tests to be performed on the portion of the memory using direct memory access (DMA) subsequent to obtaining access to the portion of the memory.

2. (Previously Presented) The computer system of claim 1 wherein the processor is configured to cause the operating system to be booted, and wherein the test module card is configured to cause the tests to be performed on the portion of the memory subsequent to the operating system being booted.

3. (Previously Presented) The computer system of claim 1 wherein the test module card is configured to cause the tests to be performed on the portion of the memory during execution of the operating system.

4. (Original) The computer system of claim 1 further comprising:

a second I/O controller coupled to the memory controller;

a second expansion slot coupled to the second I/O controller; and

an I/O device coupled to the second expansion slot.

5. (Original) The computer system of claim 1 wherein the test module card is configured to cause tests to be performed on the memory by providing read and write transactions to the first I/O controller.

6. (Original) The computer system of claim 5 wherein the read and write transactions comprise DMA transactions.

7. (Original) The computer system of claim 1 further comprising:

a bus bridge coupled to the processor and the first I/O controller.

8. (Original) The computer system of claim 1 further comprising:

a system controller that comprises the memory controller.

9. (Previously Presented) A method comprising:

obtaining access to a portion of a memory of a computer system from an operating system during operation of a computer system;

generating a test transaction in a test module card directly coupled to an expansion slot of the computer system; and

providing the test transaction to the portion using direct memory access (DMA) to cause information to be read from or stored into the portion subsequent to obtaining access to the portion of the memory.

10. (Previously Presented) The method of claim 9 further comprising:

detecting an error that occurs in response to the test transaction; and

performing a remedial action associated with the portion in response to detecting the error.

11. (Previously Presented) The method of claim 9 further comprising:

providing the test transaction from the test module to an I/O controller coupled to the expansion slot;

providing the test transaction from the I/O controller to a bus bridge;

providing the test transaction from the bus bridge to a system bus;

providing the test transaction from the system bus to a memory controller; and

providing the test transaction from the memory controller to the portion.

12. (Original) The method of claim 11 further comprising:

storing information in the memory in response to the test transaction being a write transaction.

13. (Original) The method of claim 11 further comprising:

in response to the test transaction being a read transaction:

providing information associated with the test transaction from the portion to the memory controller;

providing the information from the memory controller to the system bus;

providing the information from the system bus to the bus bridge;

providing the information from the bus bridge to the I/O controller; and

providing the information from the I/O controller to the test module.

14. (Previously Presented) The method of claim 9 further comprising:

providing the test transaction from the test module to an I/O controller coupled to the expansion slot;

providing the test transaction from the I/O controller to a system controller;

providing the test transaction from the system controller to a memory controller; and

providing the test transaction from the memory controller to the portion.

15. (Previously Presented) A computer system comprising:

a processor;

a memory controller coupled to the processor and configured to perform error correction;

a memory coupled to the memory controller;

an input/output (I/O) controller coupled to the memory controller;

an expansion slot coupled to the I/O controller; and

a test module card directly coupled to the expansion slot;

wherein the test module card is configured to obtain access to a portion of the memory from an operating system, and wherein the test module card is configured to cause tests to be performed on the portion of the memory by providing read transactions associated with the memory to the I/O controller subsequent to obtaining access to the portion of the memory.

16. (Previously Presented) The computer system of claim 15 further comprising:

the operating system;

wherein the processor is configured to cause the operating system to be booted, and wherein the test module is configured to cause the tests to be performed on the memory using DMA subsequent to the operating system being booted.

17. (Previously Presented) The computer system of claim 15 further comprising:

the operating system;

wherein the processor is configured to cause the operating system to be executed, and wherein the test module is configured to cause the tests to be performed on the memory using DMA during execution of the operating system.

18. (Previously Presented) The computer system of claim 15 wherein the I/O controller provides the read transactions to a system bus.

19. (Previously Presented) The computer system of claim 15 wherein the test module card is configured to cause tests to be performed on the memory using direct memory access (DMA).

20. (Original) The computer system of claim 15 wherein the read transactions comprise direct memory access (DMA) transactions.

## EVIDENCE APPENDIX

None.

## RELATED PROCEEDINGS APPENDIX

None.